

### IN THE CLAIMS:

Claims 1-10 are amended herein. Claims 11 and 12 are added. All pending claims are produced below. In addition, the status of each is also indicated below and appropriately noted as "Original", "Currently Amended", "Canceled", "New", "Withdrawn", "Previously Presented", and "Not Entered" as requested by the Office.

1. (Currently Amended) A method for accessing a plurality of dynamic random access memory (DRAM) devices in parallel, each device having ~~the same number of banks~~ at least one memory bank, in a parallel packet processor, the method comprising:  
partitioning a plurality of data words ~~data word~~ into data segments, the plurality of  
data words comprising a first data word and a second data word, each of the  
data segments being associated with one of the plurality of data words;  
determining a distribution of the data segments to a plurality of memory banks, the  
plurality of memory banks being among the memory banks of the plurality of  
DRAM devices, at least one data segment associated with the first word to be  
stored in parallel with at least one data segment associated with the second  
word;  
storing in parallel the data segments ~~of a data word~~ into the plurality of memory  
banks based on the distribution across a plurality of DRAM devices;  
retrieving the data segments associated with ~~of~~ a requested data word in parallel from  
the memory banks of the plurality of DRAM devices based on the  
distribution, the requested data word being one of the plurality of data words;  
and

reassembling the retrieved data segments into the requested data word.

2. (Currently Amended) The method of claim 1 further comprising:  
receiving a plurality of retrieval requests, at least one of the retrieval requests being  
associated with the requested data word, and  
wherein retrieving the data segments associated with the requested data word in  
parallel comprises retrieving the data segments associated with the requested  
data word in parallel from the memory banks of the plurality of DRAM  
devices based on the distribution, the retrieving being retrieving a plurality of  
reassembled data words in the order of the sequence that their associated in an  
order of the plurality of retrieval requests were received.
3. (Currently Amended) The method of claim 1 wherein ~~the data word~~ at least one of  
the plurality of data words has a maximum word size.
4. (Currently Amended) The method of claim 1 wherein ~~a data word~~ at least one of the  
plurality of data words includes a cell of a packet.
5. (Currently Amended) The method of claim 1 wherein ~~the data word~~ at least one of  
the plurality of data words has a fixed word size.
6. (Currently Amended) The method of claim 1 wherein ~~the data word~~ at least one of  
the plurality of data words has a variable word size.

7. (Currently Amended) The method of claim 1 wherein storing in parallel the data segments ~~of a data word~~ into the plurality of memory banks based on the distribution across a plurality of DRAM devices further comprises:  
determining an in-bank burst length based upon ~~the~~ a maximum word size, a total number of memory banks in the plurality of DRAM devices, and ~~the~~ a data width of an individual memory bank, and  
storing the ~~data word~~ data segments in a burst having the in-bank burst length.
8. (Currently Amended) The method of claim 1 wherein storing in parallel the data segments ~~of a data word~~ into the plurality of memory banks based on the distribution across a plurality of DRAM devices further comprises:  
selecting a memory bank in each of the plurality of DRAM devices ~~device~~ for each of the data segments ~~segment of the word~~, and  
storing a data segment ~~of the data word~~ in each selected memory bank in parallel, the data segment being one of the partitioned data segments.
9. (Currently Amended) The method of claim 1 further comprising scheduling the storing of the data segments independently ~~on a per~~ within a DRAM device ~~basis~~.
10. (Currently Amended) The method of claim 1 wherein retrieving the data segments associated with ~~of a~~ the requested data word in parallel ~~from banks across the DRAM devices~~ further comprises:

determining ~~the~~ a starting memory bank in each of the plurality of DRAM devices  
device storing at least one of the data segments ~~of~~ associated with the  
requested data word; and  
reading ~~each data segment of~~ data segments associated with the requested data word  
~~in each selected bank of~~ in parallel.

11. (New) A system for providing fast access to dynamic random access memory (DRAM) devices, the system comprising:  
a plurality of DRAM devices, each device having at least one memory bank;  
a chip set; and  
a memory unit comprising a persistent memory that includes microcode for execution  
by the chipset to cause the chipset to perform the operations of:  
partitioning a plurality of data words into data segments, the plurality of data  
words comprising a first data word and a second data word, each of the  
data segments being associated with one of the plurality of data words;  
determining a distribution of the data segments to a plurality of memory  
banks, the plurality of memory banks being among the memory banks  
of the plurality of DRAM devices, at least one data segment associated  
with the first word to be stored in parallel with at least one data  
segment associated with the second word;  
storing in parallel the data segments into the plurality of memory banks based  
on the distribution;

retrieving the data segments associated with a requested data word in parallel  
from the memory banks of the plurality of DRAM devices based on  
the distribution, the requested data word being one of the plurality of  
data words; and  
reassembling the retrieved data segments into the requested data word.

12. (New) The system of claim 11, wherein the persistent memory further comprises microcode for execution by the chipset to cause the chipset to perform the operation of scheduling the storing of the data segments independently within a DRAM device.